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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/013,087	12/07/2001	Hideyuki Andoh	44471-267680 (13700)	1427

23370 7590 10/21/2003

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EXAMINER

SCHILLINGER, LAURA M

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 10/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/013,087

Applicant(s)

ANDOH, HIDEYUKI

Examiner

Laura M Schillinger

Art Unit

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 August 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9, 12 and 13 is/are pending in the application.
- 4a) Of the above claim(s) 12 and 13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

**This Office Action is in response to Amendment D, dated 8/15/03 in Paper No. 12.**

#### ***Election/Restrictions***

Newly submitted claims 12 and 13 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claim 12 pertains to a device with a first main buried electrode structure and claim 13 pertains to a device such that the inner surface of the fourth semiconductor region surrounds the side boundary surface.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 12 and 13 withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Jambotkar ('857).

In reference to claim 1, Jambotkar teaches a device comprising:

A first semiconductor region of a first conductivity type, defined by a first end surface and a side boundary surface connecting the first and second end surfaces when viewed in section (Fig.2A (16));

A second semiconductor region of the first conductivity type connected with the first semiconductor region at the second end surface (Fig.2A (14));

A third semiconductor region of a second conductivity type connected with the first semiconductor region at the first end surface (Fig.2A (12)); and

A fourth semiconductor region having inner surface in contact with the side boundary surface when viewed in section and an impurity concentration lower than the first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions (Fig.2A (10)).

In reference to claim 2, Jambotkar teaches wherein the fourth semiconductor region has a first type conductivity (Fig.2A (10)).

In reference to claim 3, Jambotkar teaches wherein outer surface of the fourth semiconductor region serves as a chip outer surface of the semiconductor device and the chip outer surface is substantially orthogonal with the second end surface of the first semiconductor region.

In reference to claim 4, Jambotkar teaches wherein the fourth semiconductor region is made of a wafer cut from bulk crystal (Fig.2A (10) and Col.7, lines: 15-20).

Art Unit: 2813

In reference to claim 5, Jambotkar teaches further comprising a first main electrode layer is formed on a bottom surface of the second semiconductor region (Fig.2A (S1)).

In reference to claim 6, Jambotkar teaches wherein the first main electrode layer is contacted with the second semiconductor region, through a first concavity formed at the bottom surface of the second semiconductor region (Fig.3 (20')).

In reference to claim 7, Jambotkar teaches further comprising a first main electrode layer, a part of the first main electrode layer is buried in a via hole penetrating through the second semiconductor region, configured such that the buried part of the first main electrode layer contacts with the first semiconductor region (Fig.2A (S1)).

In reference to claim 8, Jambotkar teaches further comprising a second main electrode layer is formed on a top surface of the third semiconductor region (Fig.4A (G1)).

In reference to claim 9, Jambotkar teaches wherein the second main electrode layer is contacted with the first semiconductor regions, through a second concavity formed at the top surface of the third semiconductor region (Fig.3 (20')).

### ***Response to Arguments***

Applicant's arguments filed 7/10/03 have been fully considered but they are not persuasive. Applicant argues that Jambotkar fails to disclose a connection between the first and

Art Unit: 2813

second semiconductor regions- however this is incorrect, there is an electrical connection between the source and drain which is activated when a voltage is applied to the gate as depicted in Fig.2A (V3).

Further, Applicant argues that regions 14 and 16 never meet region 10 as claimed. However, Jambotkar teaches that the threshold voltage is related between the distance (t) demonstrated in figure A- this may be brought to "0" as described in Col.6, lines: 10-15) and therefore regions 16 and 14 will extend to meet region 10 and anticipate Applicant's claimed limitation.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Art Unit: 2813

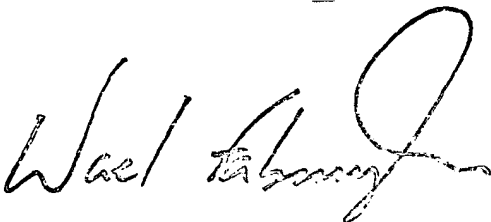
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (703) 308-6425. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (703) 308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LMS

October 18, 2003



SUPERVISORY PRIMARY EXAMINER  
TECHNOLOGY CENTER 2000